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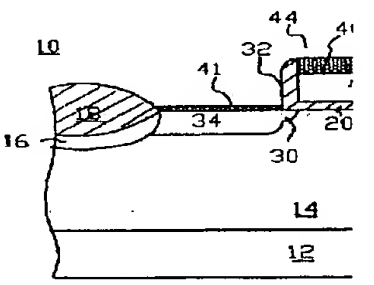
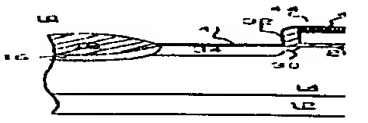
Title of invention: SELF-ALIGNMENT SILICIDE PROCESS
Abstract: PURPOSE: To form silicide different in thickness, on a
ain junction region and a gate region, by annealing a refactor
forming a first silicide layer on the gate region, and formin
icide layer on the source/drain region. CONSTITUTION: A semico
al body 10 has a P-type well 14 formed in a substrate 12. A fi
region 18 is formed over a channel stopper region 16 of option
well 14, in which a source/drain junction 34 is formed. A sil
is isolated from the surface of the P-type well 14 by a gate d
r 20. The silicide gate 44 has a silicide layer 40 and a polys
2 to which impurities are added. A side wall spacer 32 insulat
l end portion of the gate 44, and isolates junction silicide 4
T channel region.COPYRIGHT: (C)1995,JPO





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(57)
[ABSTRACT]

[PURPOSE]
On source / drain junction region and method and apparatus of the self-aligned silicide process that can make a different silicide of depthwise on a gate region are provided.
[CONSTITUTION]
A semiconductor material body comprises the well that impurities are added in in a board , on a *chiyanneru* stop domain in the well that these impurities are added in, a field insulator domain is disposed. In the well that these impurities are added in, the source / drain joining is poured. The surface of the source / drain joining is made a silicide. A silicide gate is separated from the surface of the well that impurities are added in by a gate insulating layer. A silicide gate comprises the polysilicon which the silicide layer and impurities are added in. Silicon nitride sidewall space separates sidewalls end of a silicide gate and a transistor chiyanneru domain from the source / drain joining silicide layer.

[WHAT IS CLAIMED IS]

[Claim 1]
(a) A self-aligned silicide process method to make a silicide of different depthwise on source / drain junction region and the gate region that the class of above of a refractory metal is baked, and comprise a dull *su* stage stage to make thin nitride on a source / drain region and stage that self-possession does the metal stratum of fireproof characteristics on (b) above thin nitride and a gate region and the first (c) depthwise the second assume that it is big than depthwise, and to form the class of the first silicides of the first depthwise on an above gate region and to form the class of the second silicides having the second depthwise on an above source / drain region.
[Claim 2]
(i) Sidewall space (iii) of a silicon nitride on a side wall end of a gate (ii) made a silicide having the first silicide layer of the first depthwise and an above silicide become gate and the first above depthwise the second assume that it is big than depthwise, and it is semiconductor device a self-aligned silicide comprising a transistor comprising the silicide become source / drain joining having the class of the second silicides of the second depthwise.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[INDUSTRIAL APPLICATION FIELD]
The present invention relates to production technology of if it says generally semiconductor device. Even more particularly, if it says in detail, the present invention relates to a self-aligned silicide process.

[0002]

[background art]
Because a more complicated function and requests as opposed to a higher characteristic increase in an integrated circuit, it is necessary to lower parasitism resistive element of a device structure as much as possible. It is for one method that is developed to make parasitism resistance value small to use a self-aligned silicide device structure. A conventional self-aligned silicide device structure comprises source / drain junction region and the class of small silicides of resistance value made on an insulated polysilicon gate domain. Typically, The stratum of fireproof metal such as titanium leave self-possession and reaction is done in nitrogen atmosphere. Then, Titanium responds with nitrogen, and the stratum of a titanium nitride (TiN) is formed. Even more particularly, A silicide (TiSix) is formed, on exposed silicon regions, titanium responds with silicon and and silicon is used. The stratum of TiN is removed selectively, a polysilicon gate made the source / drain joining and a silicide made a silicide having small parasitism resistive element of resistance value is made.
[0003]
A silicide usually comprises much smaller seat resistance value than the polysilicon which used impurities are added in to make a gate region of a transistor. As a result, When gate region is made a silicide , as for the silicide, a shunt does a big polysilicon of resistance value. Thus, A gate structure made a silicide has parasitism gate resistance value small by an electric shunt effect of a silicide, and and a small gate propagation delay. Even more particularly, The source / drain joining made a silicide comprises small parasitism resistance value again and, as a result, an exogenous big transconductance value is provided by a small series resistor value. Even more particularly, the source / drain joining becomes shallow to lower the short circuit *chiyanneru* effect that a drain seems to be a fall (DIBL) of a wall of evoking and a punch through leak by technology when dimensions are equal to or less than 0.5 micron. This thing limits quantity of the silicon consumption that can be permitted by a silicide of source / drain junction region. This thing gives one limit for the smallest joining depth that can be permitted again.
[0004]
A contact body process controls a leak of the joining a self-aligned (SALICIDE) process by prior art and a silicide by lowering self-possession fireproof metal depthwise to be able to leave first. However, it brings a result to produce surplus resistance value and deterioration of a transconductance value of a parasitism source / drain to make depthwise of the first fireproof metal small. In addition, Before a reaction process, an oxide layer is employed between the first titanium and silicon to improve coarseness of 2/ Ti Si Si interfaces by some another technology. However, this method comprises a weak point to introduce oxygen in silicide film. This thing is unfavorable. It , as thus described, The reason is because specific resistance of a silicide increases. Even more particularly, When, this method, a silicide thick enough is called for for high characteristic technology, surplus consumption of silicon and problems to say are not solved.
[0005]

[MEANS TO SOLVE THE PROBLEM]
If it says generally and source / drain junction region and the self-aligned silicide process

that can make a different silicide of depthwise on a gate region are disclosed by a method of one of the present invention. Thin nitride is made on a source / drain region. Next, On this thin nitride, the stratum of a refractory metal can leave self-possession. Last, The first silicide layer is made on dull shisarete, a gate region and the stratum of this refractory metal bakes, the class of the second silicides is made on a source / drain region. The first silicide layer on a gate region is thicker than the second silicide layer on a source / drain region by thin nitride.

[0006]

In an example of one of the present invention, the first dielectric layer (a gate dielectric) is made on the surface of a semiconductor material body and polysilicon the first are made on a dielectric layer. Next, The second dielectric layer is made on polysilicon. The second dielectric layer and polysilicon are etched, a polysilicon gate having sidewalls end is made. On sidewalls end of a polysilicon gate, silicon nitride sidewall space is made. In the surface of the semiconductor material body which is next to sidewall space of a device, the source / drain joining is made. A part of the first dielectric layer disposed on the source / drain joining is removed and it is moved in thin nitride. Next, The second dielectric layer is removed. On polysilicon, the first silicide layer is made and the second silicide layer is made on source / drain junction region. The second the first (a gate) silicide layer (a source / drain) is thicker than the silicide layer.

[0007]

The self-aligned silicide that independence can control depthwise of a gate silicide and depthwise of a source / drain silicide as for the advantage of one of the present invention is for a process to be provided.

[0008]

The self-aligned silicide that again another advantage of the present invention can control consumption of silicon on the source / drain joining without changing a parameter of a reaction process is for a process to be provided.

[0009]

The self-aligned silicide which can be compatible with the source / drain joining that a still another advantage is extremely light of the present invention is for a process to be provided.

[0010]

A person skilled in the art will understand these other advantages of the present invention by the following explanation that an attached drawing is referred to immediately.

[0011]

[EXAMPLE]

Drawings are different, and, in the following drawings and figures, a number to cope and a sign are referred to a supporting part unless it is declined in particular.

[0012]

It is described as a thing incorporated in N *chiyanneru* insulation gate field effect transistor (IGFET) which a process uses complementarity form metal / an oxide / a semiconductor (commercial OS) process a self-aligned silicide with the present invention, and is produced. Of course, A process can incorporate MOS in BiCMOS technology or a transistor of various kinds of forms to comprise commercial OS technology a self-aligned silicide with the present invention technically. Each of these

transistors which a process was incorporated in a self-aligned silicide with the present invention comprises an advantage in each. A general idea of the present invention can be applied to bipolar transistor technology again.

[0013]

Figure 1 is a drawing of a self-aligned silicide structure of a preferred embodiment. Semiconductor material body 10 comprises p-well 14 made in board 12. Field insulator domain 18 is posted on optional *chiyanneru* stop regions 16 in p-well 14. Field insulator domain 18 consists of an oxidation silicon material typically. However, *chiyanneru* stop domain 16 is optional, and that it is not always necessary is declined to carry out the present invention. In p-well 14, source / drain joining 34 is made. Source / drain joining 34 is an N form domain in a preferred embodiment (for the case N chiyanneru IGFET). However, source / drain joining 34 is a P form domain disposed in N form well so that it is found to a person skilled in the art immediately when a P *chiyanneru* transistor is made. This situation is possible. An advantage of one of the present invention is for it to be possible that source / drain joining 34 is light. It is because a consumption of silicon can be controlled without spoiling an IGFET gate conductivity. Thus, Various kinds of problems to accompany a short *chiyanneru* effect are relaxed.

[0014]

Gate 44 is separated from the surface of p-well 14 by gate dielectric layer 20 a silicide. Gate 44 comprises polysilicon 22 which silicide layer 40 and impurities are added in a silicide. A twist in a process is thick, and a silicide by prior art can do silicide layer 40. When it joins a source / drain with depthwise of gate silicide layer 40, and silicide 41 is made on 34 things, there is a limit to quantity of the silicon that that it is used is permitted, but , for this case, resembling is because there is not such a limit. Sidewall space 32 insulates the end where gate 44 is perpendicular, and joining silicide 41 are separated from IGFET *chiyanneru* regions. Sidewall space 32 consists of a silicon nitride in a preferred embodiment (though a polysilicon can be used again).

[0015]

FIG. 2 a is a cross-sectional view of semiconductor material body 10 comprising silicon substrate 12 after p-well 14 and *chiyanneru* stop domain 16 and field insulator domain 18 were formed. In a structure of FIG. 2 a, a process making a gate a self-aligned silicide is explained by follows.

[0016]

Gate dielectric layer 20, it is grown heat on the surface of p-well 14 by depthwise of degree of 30A - 300A (for example, 0.25 mu m technology, 60A) so that it is shown in FIG. 2 b. Other methods such as oxide self-possession to make gate dielectric layer 20 will be well known to persons skilled in the art. Next, On gate dielectric layer 20, polysilicon 22 can leave self-possession in depthwise of degree of 2000A - 4000A by chemical steam composed (CVD) technology. For example, on polysilicon 22, dielectric layer 24 can leave self-possession in depthwise of degree of 200A - 1000A by low pressure chemistry steam composed (LP CVD) technology. Other methods such as chemical steam composed (PE CVD) technology reinforced by plasma for self-possession to assume dielectric layer 24 will be well known to persons skilled in the art. Next, Dielectric layer 24 which can be removed later and polysilicon 22 are made in a pattern by microlithography and anisotropy plasma etching, polysilicon gate structure 26 shown in FIG. 2 c by it is made. A method of such an etching is well known to persons

skilled in the art.
[0017]
Drain (LDD) joining 30 that a little impurities are added in can be made with an option by ion implanter so that it is shown in FIG. 2 d. LDD joining 30 will match with polysilicon gate structure 26 and field insulator regions 18 by oneself. LDD joining 30 can be made by ion implanter after making of the first dielectric spacer (not illustrated) again. Sidewall space 32 can be made in prior art: so that it is shown in FIG. 2 e. By way of example only, Sidewall space 32 can be made self-possession does the stratum of a silicon nitride and by doing anisotropy etching. Next, On a source / drain region, a thin (50A - 100A) oxide (not illustrated) can be brought up by doing an optional oxidation stage. Next, Source / drain joining 34 (by, for example, Lin and injection of as) is made, optional thin oxide (is not illustrated) grown up is removed afterwards by oxide etching of chosen time. Source / drain joining 34 matches with sidewall space 32 and field insulator regions 18 by oneself.
[0018]
It is preferable to carry out the following process stage by means of a vacuum accumulation cluster tool. For example, an oxide layer of all nature which there is on source / drain region 34 is removed so that it is shown in FIG. 2 f and vapor phase HF at the place is used or and appropriate clearance method of low temperature is used. Afterwards, Extremely thin (for example, 8A - 40A) thermal nitride layer 36, it is grown up on a source / drain region. Nitride layer 36 can be made by short high speed thermal nitride generation (RTN) with of an ammonia atmosphere and temperature of 700 degrees Celsius - 1000 degrees Celsius during from 15 seconds to 200 seconds. In accordance with a preferred embodiment, With temperature of 700 degrees Celsius - 900 degrees Celsius, RTN is done during time of less than or equal to 60 seconds. Nitride layer 36 will comprise depthwise of 5A - around 20A. On the surface of polysilicon gate structure 26, a nitride of high density not being formed want to be attracted attention of so that there is oxide layer 24.
[0019]
For example, oxide layer 24 is removed by vapor phase HF selective etching so that it is shown in FIG. 2 g. This etching must be selective not to remove nitride layer 36. As a result, Silicon nitride sidewall space 32 will not be etched again either. Thermal nitride layer 36 comparatively comprises tolerance for etching of an oxide removal process it is high density and assume HF basics very much.
[0020]
Next, Metal layer 38 of fireproof characteristics such as titanium or cobalt uses sputter self-possession method, and, on semiconductor material body 10, it is done self-possession so that it is shown in FIG. 2 h. In accordance with a preferred embodiment, Titanium is used as a refractory metal. A self-aligned silicide process namely "a SALICIDE" process is carried out so that it is shown in FIG. 2 i. This process, Of an atmosphere to contain nitrogen, that a high-speed thermal burning condition dull *shimataha* furnace is baked, and dull *shio* is used is included. A person skilled in the art will understand that an atmosphere of ammonia (NH_3) can be used immediately. A silicide is made by silicon and reaction with refractory metal layer 38. Silicon is a few place, and refractory metal layer 38 responds with nitrogen atmosphere, a titanium nitride (TiN) is formed. Because nitride layer 36 on source / drain joining 34 is extremely light, a

nitride is become on source / drain joining 34 (than a silicide is become, straw mat). Nitride layer 36 and reaction with titanium are slow, but, the last uses a little silicon, and class of silicides 41 will be formed on source / drain joining 34. Nitride layer 36 will introduce nitrogen in silicide reaction. This thing is a very preferred thing as concerns pollution of an oxide. As a result, The source / drain joining made a silicide comprises small specific resistance than prior art and a satiny silicide / silicon interface will be comprised. Silicide layer 40 is formed by refractory metal layer 38 and reaction with polysilicon gate structure 26, making of gate 44 made a silicide by it completes. Titanium nitride (TiN) stratum 42 is made on field insulator domain 18 and source / drain region 34 made a silicide all over the period of a SALICIDE process. Titanium (not illustrated) of some non-reaction may be left on these surface again. Last, TiN layer 42 and titanium of all non-reaction use etching of choice such as *megasonikku* etching, and it is removed.
[0021]
After the method was completed, a gate and source / drain joining 34 and interconnection between things (is not illustrated) of other elements can be made in semiconductor material body 10. By way of example only, Self-possession can assume dielectric layer 46 of intermediate level in the surface of semiconductor material body 10 on the top so that it is shown in FIG. 3 a. Next, Contact body hall 58 is etched on dielectric layer 46 of intermediate level to make a contact body as opposed to source / drain joining 34 made a silicide. An interval etched with contact body hall 58, part of a silicide on source / drain joining 34 are removed again by etching. Thus, A contact body made a silicide will be preferable. Self-possession can be left on the surface so that stratum 48 of a refractory metal such as titanium is shown in FIG. 3 b. Reaction of a silicide is carried out like the above to form silicide contact body 50 on source / drain joining 34 and the surface of TiN52 so that it is shown in FIG. 3 c. Because all of refractory metal layer 48 do not respond with source / drain joining 34, silicide contact body 50 is configured at the stratum of a silicide and the stratum of TiN. Last, Stratum 60 of a conductive material such as aluminum leave self-possession on the surface of semiconductor material body 10 so that it is shown in FIG. 3 d and it is made and it is etched by a pattern. Source / drain joining 34 and interconnection between things (not illustrated) of other devices are made by it.
[0022]
surutogadekiru which makes other elements and connections between their things in semiconductor material body 10 after the method. A method to achieve this thing is well known to persons skilled in the art. Afterwards, External connections to them are done by the conducting wire joining and the direct vamp joining and them and an equal method an individual element is separated from each part of board 12 and to be well known to a person skilled in the art. Next, An individual circuit can be sealed in a dual in package, a chip carrier or package of other forms. It is disclosed by an example of one of such packages is published on January 22, 1985 and U.S. Patent No. 4,495,376 assigned by Texas *insutorumento* company.
[0023]
In the above, some preferred embodiments are disclosed in detail. It is different from the example in a range of the present invention, but, what an example to belong under a range of claim includes entirely is declined.
[0024]

The present invention is explained referring to an illustrated example, but, this is not a thing meaning that the present invention is limited to these examples. It will be found that the example that illustrated example is boiled in various ways, and was changed and the example that it is resembled in various ways, and put them together are possible from the explanation to a person skilled in the art immediately. Thus, When the present invention includes all of such a changed example, it must understand.

[0025]

The more following clauses are disclosed as concerns the above-mentioned explanation. (1) (a) A method of a self-aligned silicide process making a silicide of different depthwise on source / drain junction region and the gate region that the stratum of a refractory metal is baked, and comprise a dull $_{su}$ stage stage to make thin nitride on a source / drain region and stage that self-possession does the metal stratum of fireproof characteristics on (b) above thin nitride and a gate region and the first (c) depthwise the second assume that it is big than depthwise, and to form the class of the first silicides of the first depthwise on the gate region and to form the class of the second silicides having the second depthwise on the source / drain region.

[0026]

(2) A method of a self-aligned silicide process comprising a stage stage to remove a stage to make thin nitride on a stage to remove a stage to make the source / drain joining in the surface of the semiconductor material body which is next to a stage to make silicon nitride sidewall space on a stage to etch the dielectric cap layer and the polysilicon and a (e) above side wall end and (f) above silicon nitride sidewall space and in the first part of a (g) above gate dielectric and the first part disposed on the source / drain joining and the (h) above source / drain joining and (i) above dielectric cap layer and class of the first (j) silicides the second assume that it is thick than the class of silicides to make a stage to make dielectric cap layer on a stage to make polysilicon on a stage to make a gate dielectric on the surface of a (a) semiconductor material body and the surface of a (b) above gate dielectric and (c) above polysilicon and a polysilicon gate having a (d) side wall end, and the class of the first silicides is made on the polysilicon and to make the class of the second silicides on the source / drain region.

[0027]

(3) Stage that self-possession does the class of the first of a refractory metal on (a) above thin nitride and the nitride sidewall space and the polysilicon gate in a method as claimed in item the second and class of the first (b) silicides the second assume that it is thick than the class of silicides, and the class of the first above of a refractory metal is baked of an atmosphere to contain nitrogen to make the class of the first of a silicide on the polysilicon gate, and it is dull shi and the method how the class of the second and class of the first of the nitride sidewall space and refractory metal nitride are baked, and the stage to make the class of the first silicides and the class of the second silicides comprises a dull $_{su}$ stage and a stage to remove the class of the first of a (c) refractory metal nitride of a silicide.

[0028]

(4) In a method as claimed in item the third, the first above layer of a refractory metal is the methods having titanium. (5) In a method as claimed in item the second, the first silicide layer and the second silicide layer are the methods made at a reaction stage one silicide. (6) In a method as claimed in item the second, the stage to make the dielectric

cap layer is 200A, there is, and it is done, and it is the method having an LP CVD oxide layer self-possession stage having depthwise in the range of 500A. (7) The method, even more particularly, to comprise a stage to make a drain containing a little impurities before the stage to make the silicon nitride sidewall space in a method as claimed in item the second.

[0029]

(8) In a method as claimed in item the second, the stage to make the thin nitride is the method having a stage nitrogen compounds of heat to be rapid of an ammonia atmosphere of 700 degrees Celsius - 1000 degrees Celsius for from 15 seconds to 200 seconds. (9) In a method as claimed in item the second, the thin nitride is the process methods having depthwise in the range of 5A - 20A. (10) The method, even more particularly, to comprise a stage to make several interconnection Line to connect to a stage to make an each silicide contact body on a stage to etch part of the interlevel dielectric layer on a stage to make a dielectric layer of intermediate level on the semiconductor material body after the first (a) above nitride layer and the stage to make the second nitride layer and the (b) above source / drain joining and the (c) above source / drain joining and a (d) above silicide contact body in a method as claimed in item the second. (11) The method the class of the second above of a refractory metal is baked of an atmosphere to contain nitrogen, and to comprise a dull $_{SU}$ stage the stage to make the silicide contact body makes the third stratum of a silicide on the stage that self-possession does the class of the second of a refractory metal and the (b) above source / drain joining on a (a) above interlevel dielectric layer and the source / drain joining and to make the second stratum of a titanium nitride on the interlevel dielectric layer in a method as claimed in item the tenth.

[0030]

(12) *(Fail: -1000:::: This sentence faied in the transration.)*

[0031]

(13) In a method as claimed in item the twelfth, the first above layer of a refractory metal is the methods having titanium. (14) In a method as claimed in item the twelfth, the stage to make the thin nitride is the method having a stage rapid nitrogen compounds for from 15 seconds to 200 seconds of an ammonia atmosphere of 700 degrees Celsius - 1000 degrees Celsius. (15) The method, even more particularly, to comprise a stage to make several interconnection Line to a stage to make an each silicide contact body on a stage to etch part of the interlevel dielectric layer on a stage to make a dielectric layer of intermediate level on the semiconductor material body after the first (a) above silicide layer and the stage to make the class of the second silicides and (b) above source / drain junction region and (c) above source / drain junction region and a (d) above silicide contact body in a method as claimed in item the twelfth.

[0032]

(16) (i) sidewall space (iii) of a silicon nitride on a side wall end of a gate (ii) made a silicide having the first silicide layer of the first depthwise and an above silicide become gate and the first above depthwise the second assume that it is big than depthwise, and it is semiconductor device a self-aligned silicide comprising a transistor comprising the silicide become source / drain joining having the class of the second silicides of the second depthwise. (17) The device which is field effect transition of the gate that the transistor is insulated in a device as claimed in item the 16th. (18) The device that the

silicide layer is titanium silicide in a device as claimed in item the 16th. (19) The device it is disposed on a silicide contact body disposed on an interlevel dielectric layer disposed on a (a) above transistor and the (b) above source / drain joining and a (c) above interlevel dielectric layer in a device as claimed in item the 16th and, even more particularly, comprise the class of silicides and interconnection Line touching electrically.
[0033]
(20) The self-aligned silicide process when different silicide depthwise is possible is disclosed for a polysilicon gate and source / drain junction region. Semiconductor material body 10 comprises well 14 that impurities are added in in board 12. On *chiyanneru* stop domain 16 in well 14 that these impurities are added in, field insulator domain 18 is posted. In well 14 that impurities are added in, source / drain joining 34 is poured. Source / drain joining 34 is the slight regions which impurities are added in abundantly. The surface of source / drain joining 34 is made a silicide. Silicide gate 44 is separated from the surface of well 14 that impurities are added in by gate insulating layer 20. Silicide gate 44 comprises polysilicon 22 which silicide layer 40 and impurities are added in. Depthwise of silicide layer 40 needs not to be limited by quantity of silicon used on by surface depthwise made a silicide of source / drain joining 34 or a thing of these joining. Silicon nitride sidewall space 32 separates sidewalls end of silicide gate 44 and a transistor chiyanneru domain from source / drain joining silicide layer 41.

[BRIEF DESCRIPTION OF DRAWINGS]

[FIG. 1]
A self-aligned silicide by preferred embodiment to the present invention is a cross-sectional view of a structure.
[FIG. 2]
It is a cross-sectional view of a manufacturing process of preferred embodiment to the present invention, and a-i is a transverse cross-sectional view of a consecutive stage of a manufacturing process.
[FIG. 3]
It is a cross-sectional view of a manufacturing process of preferred embodiment to the present invention, and a-d is a device contact body and a cross-sectional view of a consecutive stage of a manufacturing process of an interconnect.
[DENOTATION OF REFERENCE NUMERALS]
44 class of 41 class of 32 34 40 polysilicon sidewall space source / drain joining silicides source / drain silicides silicide gates that 16 18 20 22 well *chiyanneru* stop domain field insulator domain gate insulating layer impurities which ten 12 14 semiconductor material body board impurities are added in are doped

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